WHAT IS CLAIMED IS:

1. A Boundary-Scan test receiver for capturing signals during board interconnect testing, comprising:

   a) a comparator comprising a first input to receive said signals during board interconnect testing, and a second input to receive a reference voltage; and

   b) a programmable hysteresis circuit coupled to at least one of said comparator inputs.

2. The Boundary-Scan test receiver of claim 1, wherein the programmable hysteresis circuit comprises a programmable hysteresis voltage generator.

3. The Boundary-Scan test receiver of claim 2, wherein the programmable hysteresis voltage generator comprises a current digital-to-analog converter to sink current from one of said first and second inputs.

4. The Boundary-Scan test receiver of claim 1, wherein the programmable hysteresis circuit comprises a programmable hysteresis delay circuit.

5. The Boundary-Scan test receiver of claim 4, wherein the programmable hysteresis delay circuit comprises a digital-to-analog converter driving a plurality of variable capacitances, the capacitances being coupled at various points along a chain of buffer elements.

6. The Boundary-Scan test receiver of claim 4, wherein the programmable hysteresis delay circuit comprises a digital-to-analog converter driving a chain of switchable delay elements.

7. The Boundary-Scan test receiver of claim 1, wherein programmable inputs of the hysteresis circuit are linked in a scan chain.

8. A Boundary-Scan test receiver for capturing signals during board interconnect testing, comprising:

a) a plurality of comparators, each comprising a first input to receive said signals during board interconnect testing, and a second input to receive a reference voltage; and

b) a programmable hysteresis circuit coupled to at least one input of each comparator.

9. The Boundary-Scan test receiver of claim 8, wherein the programmable hysteresis circuit comprises a programmable hysteresis voltage generator; the programmable hysteresis voltage generator comprising:

a) a voltage divider, coupled between an input of each comparator;

b) a current digital-to-analog converter driving the voltage divider; and

c) a current mirror, coupled to a midpoint of the voltage divider to mirror a reference voltage at said midpoint.

10. The Boundary-Scan test receiver of claim 8, wherein the programmable hysteresis circuit comprises a programmable hysteresis voltage generator; the programmable hysteresis voltage generator comprising:

a) a voltage divider, coupled between an input of each comparator;

b) a current digital-to-analog converter driving the voltage divider; and

c) a current mirror, coupled to a midpoint of the voltage divider to mirror a common mode voltage of said signals at said midpoint.

11. A Boundary-Scan test method, comprising:

a) determining at least one operating condition of a board under test;

b) in response to said determined operating conditions, programming hysteresis circuits of Boundary-Scan test receivers in the board under test; and

c) executing a Boundary-Scan test.

12. The Boundary-Scan test method of claim 11, wherein determining the at least one operating condition comprises determining a signaling level of a component of the board under test.

13. The Boundary-Scan test method of claim 11, wherein determining the at least one operating condition comprises determining a noise level associated with signal paths of the board under test.

14. The Boundary-Scan test method of claim 13, further comprising, prior to determining the at least one operating condition:

a) programming hysteresis circuits of the Boundary-Scan test receivers with default values; and

b) executing a Boundary-Scan test;

wherein determining the noise level associated with signal paths of the board under test comprises evaluating results of the Boundary-Scan test ran with the default values.

15. The Boundary-Scan test method of claim 11, further comprising, prior to determining the at least one operating condition:

a) programming hysteresis circuits of the Boundary-Scan test receivers with default values; and

b) executing a Boundary-Scan test;

wherein determining the at least one operation condition of the board under test comprises evaluating results of the Boundary-Scan test ran with the default values.

16. The Boundary-Scan test method of claim 11, wherein programming the hysteresis circuits comprises programming a hysteresis voltage.

17. The Boundary-Scan test method of claim 11, wherein programming the hysteresis circuits comprises programming a hysteresis delay.

18. The Boundary-Scan test method of claim 11, wherein hysteresis circuits of a component of the board under test are programmed via bits shifted through a scan chain.

19. The Boundary-Scan test method of claim 18, wherein the hysteresis circuits of the component of the board under test are programmed in a plurality of sets.